**1.)**

The previous design utilized a referential input, as can be seen in figure 1. The input channels labeled “IN\_CH64 – IN\_CH57” are the positive inputs (INxP, pins 2,4,6,8,10,12,14,16) that go into the ADS1299. The negative inputs (INxN, 1,3,5,7,9,11,13,15) are being grounded. In figure 2, we can see the recommended layout given by the datasheet of the ADS1299. According to the datasheet there needs to be low pass filtering between each positive input and the SRB1, which acts as the reference electrode. The previous design doesn’t have low pass filtering, nor the referencing into SRB1 pin.



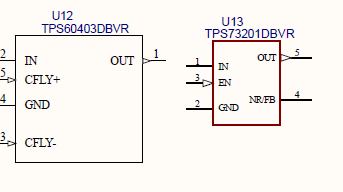
**Figure 1**. Previous Schematic Design



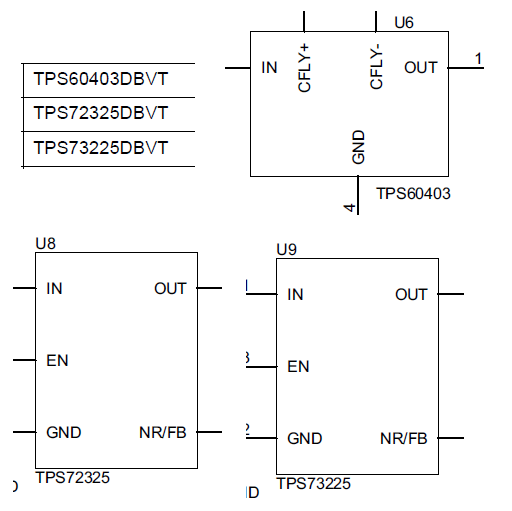
**Figure 2**. Referential Montage, page 67 of ADS1299 datasheet

**2.)**

The previous design also utilized a different type of regulator as recommended within the datasheet of the EEG Front-End Performance Demonstration Kit. Figure 3 shows the type of regulator used within the previous design. Figure 4 shows the regulators recommended. The regulators used within the previous design are —TPS73201— and they placed them for both of the voltage values —+2.5V and -2.5V—. Within the datasheet it states to us —TPS72325 & TPS73225— one for each voltage. Also, the type of the TPS60403 is different as well. The difference are negligible, however the datasheet recommends these specific types and therefore should be used.



**Figure 3**. Previous design regulators for power supply



**Figure 4.** Power supply regulators, page 52 & 58 of EEG Front-End Datasheet

**3.)**

Within the previous design there are connections with capacitors in the regulator output of the power supply schematics. Figure 5 shows the previous design. The capacitor C207 (0.01uF) is being connected to pin 5 and pin 4 of the regulator TPS73201DBVR, which recommended within the “tsp732” datasheet. However, Figure 6 it recommends a layout given by the datasheet of the EEG Front-End Performance Demonstration Kit. Capacitor C67 is representing the same capacitor within the previous design. We can see that the capacitor isn’t to be connected to pins 4 and 5. It should only be connected to pin 4 and then analog grounded. This was also present in every regulator that uses the TPS73201DBVR.



**Figure 5.** Previous design of power supply regulator output



**Figure 6.** Power supply regulator output, page 52 of EEG Front-End datasheet

**4.)**

According to the EEG Front-End Performance Demonstration Kit datasheet page 14. Figure 7 is a screen shot of a paragraph from the datasheet where it states that the voltages for DVDD should be within +1.8 - +3.0V. However, in figure 8 shows the previous schematic and it’s expecting an output voltage of +3.3V. Figure 9 shows the limits of the ADS1299 according to its datasheet. Though the voltage ranges of the ADS1299 can handle +1.8 to +3.6V. However, within figure 10 we can see that there are protentional input currents and a +0.3V to DVDD should be added into the design. Therefore, based on this the original circuit could potential have a +3.6V on DVDD. This is at maximum and may cause issues.



**Figure 7.** limit of Digital voltages for the ADS1299



**Figure 8.** Previous DVDD voltage design



**Figure 9.** Limits of Digital voltages based on ADS1299 datasheet



**Figure 10.** Potential input currents